



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,944	08/20/2003	Yoshiaki Hasegawa	63979-032	3843

7590 10/27/2006
McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

VAN ROY, TOD THOMAS

ART UNIT	PAPER NUMBER
----------	--------------

2828

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/643,944	Applicant(s) HASEGAWA ET AL.	
	Examiner Tod T. Van Roy	Art Unit 2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-7 and 9-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6,7 and 9-14 is/are allowed.
- 6) ☒ Claim(s) 1,3-5,15-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>10/13/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The examiner acknowledges the amending of claims 1 and 5, and the addition of claims 16-23.

Response to Arguments

Applicant's arguments with respect to claims 1, and 5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Art Unit: 2828

Claims 1, 3-5, and 16- 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (JP 11-251687, applicant submitted prior art) in view of Ikeda (US 6111277).

With respect to claim 1, Hasegawa teaches a semiconductor laser in which an n-type semiconductor layer (fig.1a #13), an active layer (fig.1a #15), and a p-type semiconductor layer are stacked in this order on a substrate (fig.1a #10); the active layer comprising a well layer composed of InGaN (fig.1a #15 abs.); the semiconductor laser comprising an intermediate layer sandwiched between the active layer and the p-type semiconductor layer (fig.1a #16); the intermediate layer including no intentionally added impurities and being composed of a gallium nitride-based compound semiconductor (abs., [0029], no impurities taught in the layer formation); the intermediate layer being composed of GaN or InGaN (GaN, abs.); and with no p-type semiconductor layer being present between the active layer and the intermediate layer. Hasegawa does not teach a semiconductor layer between the substrate and the n-type semiconductor layer having a threading dislocation density of not more than $5 \times 10^8 \text{cm}^{-2}$. Ikeda teaches a nitride semiconductor device having a layer (fig.2 #3) between the substrate (fig.2 #1) and the first n-type layer (fig.2 #6) which has a threading dislocation density of less than $5 \times 10^8 \text{cm}^{-2}$ (col.4 lines 20-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the nitride device of Hasegawa with the layer and low dislocation density of Ikeda in order to create a buffer region that reduces dislocation density throughout the device.

With respect to claim 3, Hasegawa teaches the semiconductor laser is a Group III-V nitride semiconductor laser (abs.), the n-type semiconductor layer contains Si as an n-type impurity ([0028]), and the p-type semiconductor layer contains Mg as a p-type impurity ([0030]).

With respect to claim 4, Hasegawa teaches the concentration of a p-type impurity in the active layer is about $1\text{E}17\text{ cm}^{-3}$ or lower ([0029], no added impurities, so is lower).

With respect to claim 5, Hasegawa teaches forming the device as outlined in the rejection to claim 1 ([0026-32]). Hasegawa does not teach forming a semiconductor layer between the substrate and the n-type semiconductor layer having a threading dislocation density of not more than $5\text{E}8\text{cm}^{-2}$. Ikeda teaches a nitride semiconductor device having a layer (fig.2 #3) between the substrate (fig.2 #1) and the first n-type layer (fig.2 #6) which has a threading dislocation density of less than $5\text{E}8\text{cm}^{-2}$ (col.4 lines 20-26). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the nitride device of Hasegawa with the layer and low dislocation density of Ikeda in order to create a buffer region that reduces dislocation density throughout the device.

With respect to claim 15, Hasegawa teaches the thickness of the intermediate layer is not less than 60nm and not more than 160nm ([0029], 100nm).

With respect to claims 18 and 21, Hasegawa and Ikeda teach the nitride device outlined in the rejection to claim 1, when Ikeda further teaches forming the buffer layers by using a stripe-like insulating pattern (fig.2 #4a) and growing a semiconductor layer

Art Unit: 2828

between and over the lines (fig.2 #5a), the semiconductor layer having low dislocation densities over the insulating pattern and higher dislocation densities between the patterns (as seen in fig.2).

With respect to claims 16 and 19, Hasegawa and Ikeda teach the nitride devices outlined in the rejections to claims 1 and 18 above, and Hasegawa further teaches the p-type layer (and all cited doped layers) to be in a ridge-type form that would be immediately over the low dislocation regions.

With respect to claims 17 and 20, Ikeda further teaches the n-type doping of the barrier layers ([0036]). The use of doping of the barriers is known in the art to be used with laser active regions (demonstrated by Ikeda). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the barrier layer doping of the known materials, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960).

Claims 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa and Ikeda in view of Northrup et al. (US 2003/0091085).

With respect to claims 22-23, Hasegawa and Ikeda teach the nitride device outlined in the rejection to claim 1, but do not teach the undoped GaN waveguiding intermediate layer to be composed of InGa_N. Northrup teaches a nitride device wherein a waveguiding layer is taught to be composed of either GaN or InGa_N ([0036]) and is

Art Unit: 2828

undoped. It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the undoped GaN waveguiding layer of Hasegawa with the undoped InGaN waveguiding layer of Northrup in order to tailor the bandgap and lattice constant in the vicinity of the active region, influencing both carrier confinement and strain features.

A reference noted, but not relied upon, is that of Itaya et al. (US 5903017). Itaya teaches a nitride device wherein it is taught that incorporation of Indium into GaN allows for tailoring of the bandgap (col.2 lines 30-42).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2828

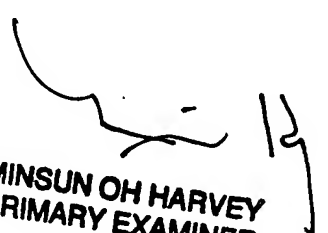
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR


MINSUN OH HARVEY
PRIMARY EXAMINER